IN THE SPECIFICATION:

Please amend paragraph **[0001]** as follows:

[0001] This application is a continuation of application Serial No. 08/609,354, filed March 1, 1996, ~~which is~~ now United States Patent No. 6,825,596, issued November 30, 2004, which is a divisional of application Serial No. 08/089,166, filed July 7, 1993, ~~which is~~ now United States Patent No. 5,532,177, issued July 2, 1996. There is a continuation application having Serial No. 08/555,908, ~~which was~~ filed on November 13, 1995, now abandoned. That ~~copending~~ application is a continuation of application Serial No. 08/089,166, ~~which was~~ filed on July 7, 1993 and issued as United States Patent No. 5,532,177 on July 2, 1996. Also, there is a divisional of application Serial No. 08/609,354, which was filed on September 25, 1998 as application Serial No. 09/161,338, now United States Patent No. 6,049,089 issued April 11, 2000.

Please amend paragraph **[0003]** as follows:

[0003] Background of the Invention: Cathode ray tube (CRT) displays, such as those commonly used in ~~desk-top~~ desktop computer screens, function as a result of a scanning electron beam from an electron gun impinging on phosphors on a relatively distant screen. The electrons increase the energy level of the phosphors. The phosphors release energy imparted to them from the bombarding electrons, thereby emitting photons, which photons are transmitted through the glass screen of the display to the viewer.

Please amend paragraph **[0005]** as follows:

[0005] In U.S. Patent No. 3,875,442, entitled "Display Panel," Wasa ~~et. al.~~ et al., disclose a display panel comprising a transparent gas-tight envelope, two main planar electrodes ~~which~~ that are arranged within the gas-tight envelope parallel with each other, and a cathode luminescent panel. One of the two main electrodes is a cold cathode, and the other is a low potential anode, gate, or grid. The cathode luminescent panel may consist of a transparent glass plate, a transparent electrode formed on the transparent glass plate, and a phosphor layer coated

on the transparent electrode. The phosphor layer is made of, for example, zinc oxide which can be excited with ~~low-energy~~ low-energy electrons.

Please amend paragraph **[0006]** as follows:

[0006] ~~Spindt, et. al.~~ Spindt et al., discuss field emission cathode structures in U.S. Patent Nos. 3,665,241; 3,755,704; 3,812,559; and 4,874,981. To produce the desired field emission, a potential source is provided with its positive terminal connected to the gate, or grid, and its negative terminal connected to the emitter electrode (cathode conductor substrate). The potential source may be made variable for the purpose of controlling the electron emission current. Upon application of a potential between the electrodes, an electric field is established between the emitter tips and the grid, thus causing electrons to be emitted from the cathode tips through the holes in the grid electrode.

Please amend paragraph **[0010]** as follows:

[0010] In the process of the present invention, a dopant material ~~which~~ that affects the oxidation rate or the etch rate of silicon is diffused into a silicon substrate or film. "Stalks" or "pillars" are then etched, and the dopant differential is used to produce a sharpened tip. Alternatively, "fins" or "hedges" may be etched, and the dopant differential used to produce a sharpened edge.

Please amend paragraph **[0013]** as follows:

[0013] Figure 1 is a schematic ~~crosssection~~ cross-section of a field emission device in which the emitter tips or edges formed from the process of the present invention can be used;

Please amend paragraph **[0014]** as follows:

[0014] Figure 2 ~~(FIG. 2)~~ is a schematic cross-section of the doped substrate of the present invention superjacent to which is a mask, which in this ~~embodiment~~ embodiment, comprises several layers;

Please amend paragraph **[0016]** as follows:

[0016] Figure 4 is a schematic cross-section of the substrate of Figure 3, after the tips or edges have been formed according to the process of the present invention; ~~and~~

Please amend paragraph **[0017]** as follows:

[0017] Figure 5 is a schematic cross-section of the tips or edges of Figure 4, after the nitride and oxide layers of the mask have been ~~removed.~~ removed; and

Please amend paragraph **[0017A]** as follows:

[0017A] Figure 5A is a schematic cross-section of the tips or edges of Figure 4A, after the nitride and oxide layers of the mask have been ~~removed;~~ removed.

Please amend paragraph **[0020]** as follows:

[0020] Figure 1 ~~(FIG. 1)~~ is merely illustrative of the many applications for which the emitter 13 of the present invention can be used. The present invention is described herein with respect to field emitter displays, but one having ordinary skill in the art will realize that it is equally applicable to any other device or structure employing a micro-machined point, edge, or blade, such as, but not limited to, a stylus, probe tip, fastener, or fine needle.

Please amend paragraph **[0023]** as follows:

[0023] At a field emission site, a micro-cathode 13 (also referred to herein as an emitter) has been constructed in the substrate 11. The micro-cathode 13 is a protuberance ~~which~~ that may have a variety of shapes, such as pyramidal, conical, wedge, or other ~~geometry~~ geometry, which has a fine micro-point, edge, or blade for the emission of electrons. The micro-cathode 13 has an apex and a base. The aspect ratio (i.e., height-to-base width ratio) of the emitters 13 is preferably greater than 1:1. Hence, the preferred emitters 13 have a tall, narrow appearance.

Please amend paragraph **[0026]** as follows:

[0026] The electron emitter 13 is integral with the semiconductor substrate 11 and serves as a cathode conductor. Gate structure 15 serves ~~as and~~ as an extraction grid for its respective micro-cathode 13. A dielectric insulating layer 14 is deposited on the substrate 11. However, a conductive cathode layer (not shown) may also be disposed between the dielectric insulating layer 14 and the substrate 11, depending upon the material selected for the substrate 11. The dielectric insulating layer 14 also has an opening at the field emission site location.

Please amend paragraph **[0028]** as follows:

[0028] Figure 2 ~~(FIG. 2)~~ shows the substrate or film 11 which is used to fabricate a field emitter 13. The substrate 11 is preferably single crystal silicon. An impurity concentration gradient 13A is introduced into the substrate or film 11 in such a manner so as to create a concentration gradient from the top of the substrate 11 ~~surface~~ surface, which decreases with depth down into the film or substrate 11. Preferably, the impurity concentration gradient 13A is from the group including, but not limited to, boron, phosphorus, and arsenic.

Please amend paragraph **[0028A]** as follows:

[0028A] Figure 2A ~~(FIG. 2A)~~ shows the substrate or film 11 which is used to fabricate a field emitter 13. The substrate 11 is preferably single crystal silicon. An impurity ~~material~~ concentration gradient 13A′ is introduced into the substrate or film 11 in such a manner so as to create a concentration gradient from the top of the substrate ~~surface 11~~ 11 surface, which increases with depth down into the film or substrate 11. Preferably, the impurity concentration gradient 13A′ is from the group including, but not limited to boron, phosphorus, and arsenic.

Please amend paragraph **[0030]** as follows:

[0030] In the case of a CVD or epitaxially grown film, it is possible to introduce an impurity ~~which~~ that decreases throughout the deposition and serves as a component for retarding the consumptive process subsequently employed in the process of the present invention. An example is the combination of a silicon film or substrate 11, doped with a boron impurity concentration gradient 13A, and etched with an ethylene diamine pyrocatechol (EDP) etchant, where the EDP is employed after anisotropically etching pillars or fins from substrate 11.

Please amend paragraph **[0031]** as follows:

[0031] In the preferred embodiment, the substrate 11 is single crystal silicon. After doping, the film or substrate 11 is then patterned, preferably with a resist/silicon nitride/silicon oxide sandwich etch mask 24 and dry etched. Other types of materials can be used to form the sandwich etch mask 24, as long as they provide the necessary selectivity to the substrate 11. The resist/silicon nitride/silicon oxide sandwich etch mask 24 has been selected due to its tendency to assist in controlling the lateral consumption of silicon during thermal oxidation, which is well known in semiconductor LOCOS (Local Oxidation of Silicon) processing.

Please amend paragraph **[0032]** as follows:

[0032] The structure of Figure 2 ~~(FIG. 2)~~ is then etched, preferably using a reactive ion, crystallographic etch, or other etch method well known in the art. Preferably, the etch is substantially anisotropic, i.e., having undercutting ~~which~~ that is reduced and controlled, thereby forming "pillars" in the substrate 11, which "pillars" ~~are depicted in Figure 3 (FIG.3) and~~ will be the sites of the emitter tips 13 of the present invention.

Please amend paragraph **[0032A]** as follows:

~~[0032A]~~ **[0032A]** The structure of Figure 2A ~~(FIG 2A)~~ is then etched, preferably using a reactive ion, crystallographic etch, or other etch method well known in the art. Preferably, the etch is substantially anisotropic, i.e., having undercutting that is reduced and controlled, thereby

forming ~~"pillars"~~ pillars 50 in the substrate 11, which ~~"pillars"~~ pillars 50 are depicted in Figure 3A ~~(FIG 3A)~~ and will be the sites of the emitter tips 13 of the present invention.

Please amend paragraph **[0033]** as follows:

[0033] Figure 4 ~~(FIG. 4)~~ illustrates the substrate 11 having emitter tips 13 formed therein. The resist portion 24A ~~(FIG.~~ (Figure 2) of the sandwich etch mask 24 has been removed. An oxidation is then performed, wherein an oxide layer 25 is disposed about the emitter tip 13 and subsequently removed.

Please amend paragraph **[0033A]** as follows:

[0033A] Figure 4A ~~(FIG. 4A)~~ illustrates the substrate 11 having emitter tips 13 formed therein. The resist portion 24A ~~(FIG.~~ (Figure 2A) of the sandwich etch mask 24 has been removed. An oxidation is then performed, wherein an oxide layer 25 is disposed about the emitter tip 13 and subsequently removed.

Please amend paragraph **[0036]** as follows:

[0036] The etch is preferably nondirectional in nature, removing material of a selected purity level in both horizontal and vertical directions, thereby creating an undercut. The amount of undercut is related to the impurity concentration gradient 13A, 13A'.

Please amend paragraph **[0037]** as follows:

[0037] Figure 5 ~~(FIG.5)~~ shows the emitters 13 following the removal of the nitride 24B and oxide 24C layers (shown in ~~FIG. 2~~ Figures 2-4); preferably by a selective wet stripping process. An example of such a stripping process involves a 1:100 solution of hydrofluoric acid (HF)/water at 20° C, followed by a water rinse. Next is a boiling phosphoric acid (H_3PO_4)/water solution at 140° C, followed by a water rinse and a 1:4 hydrofluoric acid (HF)/water solution at 20° C. The emitters 13 of the present invention are thereby exposed.

Please amend paragraph **[0037A]** as follows:

[0037A] Figure 5A ~~(FIG. 5A)~~ shows the emitters 13 following the removal of the nitride 24B and oxide 24C layers (shown in ~~FIG.~~ Figure 2A); preferably by a selective wet stripping process. An example of such a stripping process involves a 1:100 solution of hydrofluoric acid (HF)/water at 20° C, followed by a water rinse. Next is a boiling phosphoric acid (H_3PO_4)/water solution at 140° C, followed by a water rinse and a 1:4 hydrofluoric acid (HF)/water solution at 20° C. The emitters 13 of the present invention are thereby exposed.